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WAFER BURN-IN TEST CIRCUIT FOR SEMICONDUCTOR MEMORY

## Abstract:

PROBLEM TO BE SOLVED: To form various back ground writing patterns for preventing a load exceeding the withstand voltage from being applied to a transistor by providing subword line drivers for enabling word lines according to word line activating signals, etc.

SOLUTION: Word lines WL0-WL3 are connected to corresponding word line activating signals PXD

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